THERMAL RESISTANCE OF InGaAs/InP LASER DIODES

W. Both and J. Piprek

CENTRAL INSTITUTE OF OPTICS AND SPECTROSCOPY RUDOWER CHAUSSEE 6, BERLIN VEB WERK FÜR FERNSEHELEKTRONIK OSTENDSTR. 1 - 14, BERLIN, GERMANY

(Received February 10, 1990)

Results of theoretical and experimental investigations of the thermal behaviour of InGa-AsP/InP laser diodes with a ridge-waveguide structure are presented. It is shown that, in contrast to GaAlAs/GaAs laser diodes, most of the heat flux is carried through the InP-substrate, less than 1/4 through the ridge. The temperature rise in the active region was determined and the thermal resistance calculated for various structure and bond parameters. The theoretical and experimental results fit very well. The change of the thermal resistance compared to a norm value of 67 K/W with variation of structure parameters is discussed. It is strongly affected by the device length, the ridge width and the bonding parameters.

Because of the better transmission properties of optical fibres in the 1.3 - $1.55 \,\mu$ m wavelength range laser diodes based on InGaAsP/InP are favoured as optical transmitters. For optical fibre communication devices with high reliability, low threshold current and high frequency stability are demanded. Especially index-guided laser structures seem useful. We investigated the thermal behaviour of a quasi-index-guided laser structure [1]. The relatively simple technology based on common epitaxy with the simultaneous fabrication of mode and current confinement in a ridge is an advantage compared to more complicated index-guided structures.

One of the main problems of laser diodes in operation is the temperature in the active region. In laser diodes based on InGaAsP/InP the threshold current is very temperature sensitive. It is expressed in the T_0 -value.

$$I_{th} (T + \Delta T) = I_{th} (T) \exp (\Delta T/T_0)$$
(1)

While in GaAlAs/GaAs double heterostructures (DHS) the T_0 -value is in the range of 150 - 200 K, for InGaAsP/InP DHS T_0 -values of 50-70 K are typical.

John Wiley & Sons, Limited, Chichester Akadémiai Kiadó, Budapest So it seems necessary to study the thermal loading of InGaAsP/InP-laser diodes under operating conditions. We investigated both theoretically and experimentally the temperature distribution in a chip and the thermal resistance with the variation of various structure parameters.

Structure parameters

To achieve a good confinement of light and current a mesa is etched out of the epitaxial structure. The channels were covered with an insulator. Only the top of the ridge is used as an electrical contact. The chips were mounted p-side-down on a copper heatsink by soldering. In Fig. 1 the structure of the OCMR-(Oxide-Clad-Mesa Ridge) laser diode is shown schematically. The typical structure parameters (used for normalization) are given in Table 1.

The typical ridge width w is $5/\mu$ m and the channel width $C = 22.5 \ \mu$ m. The device length is $L = 200 \ \mu$ m. The voltage drop at the *p*-*n*-junction is typically $U_a = 1$ V. The ambient temperature for both modelling and measurement was 25° . More data about parameters and application are presented in [1].



Fig. 1 Scheme of the Oxide-Clad-Mesa-Ridge- (OCMR) laser diode

Layer Nr.	Material	Thickness µm	Thermal cond., W/Km
1	Solder	10	25 [2]
2	Ti/Au-contact	0.2	300
3	Isolator	0.2	2
4	Contact layer	0.6	4.8 [3]
5	p-InP layer	1.3	88 [3]
6	etch stop layer	0.3	5.9 [3]
7	active region	0.2	4.3 [3]
5	InP-substrate	100	88 [3]

Table 1 Typical parameters of the investigated OCMR-structure

Theory

1. Model for temperature calculations

The temperature distribution T(x, y) perpendicular to the ridge is obtained as solution of the stationary thermal conduction equation

$$- \operatorname{div} \left[\lambda \left(x, y\right)\right] \quad \operatorname{grad} \quad T(x, y) = \partial P / \partial V \left(x, y\right) \tag{2}$$

Boundary conditions are given by

$$T |_{sink} = T_s \text{ and } \partial T / \partial \nu |_{air} = 0$$
(3)

assuming the surface temperature T_s of the heat sink as homogeneous and neglecting heat flux to the air around the chip $(\partial T / \partial v$ -normal derivative). Both inside the different layers and within the temperature variations the thermal conductivity $\lambda(x, y)$ can be taken as constant. In the active region a uniform heat power density is approximated by

$$\partial P / \partial V |_{active \ region} = IU_a / V_a$$
 (4)

where I, U_a and V_a are the average current, the voltage drop and the volume of the active region. Eq. (4) neglects the relatively small value of radiation powerin the active regions. This simple attempt is justified, because in the analysis calculated temperatures will be transformed into material parameters which are independent of heat power values. Joule heating in each layer depends on the local current density and on the electrical resistivity of the corresponding material. Usually, only the metal-semiconductor contact on the top of the ridge exhibits an appreciable electrical resistance up to $R_z = 10 \Omega$ connected with the power density of this second heat source

$$\frac{\partial P}{\partial V}|_{contact} = I^2 R / V_c \tag{5}$$

using the full volume V_c of the Ti/Au-layer because of its high thermal conductivity.

This two-dimensional model excludes heat transfer along the z-axis and for that reason heat sources at the mirrors of the active region cannot be taken into account.

The differential Eq. (2) is solved numerically by PLTMG, a piecewise linear triangular multigrid finite element code [4]. Device symmetry permits reducing the calculations on one half of the chip cross section only. The heat sink temperature T_s is 25°, the resulting distribution T(x, y) can easily be related to other values T_s . The heat power generated in the active region ($P_a = U_a I$) and in the contact ($P_c = R_c I^2$), respectively, is assumed as 100 mW.

Results of model calculations

Temperature and thermal resistance

Considering the parameters reported above, the computed temperature distribution T(x, y) is presented in Fig. 2 for the half cross section of the device and in Fig. 3 as enlargement of the ridge region. The maximum temperature of 37.4° occurs in the Ti/Au-contact layer. Inside the active width region the maximum value $T_a^{max} = 35.7^{\circ}$ is located in the middle of the active regions interface to the etch stopping layer. Perpendicular to this interface the temperature goes down to 33.8° inside the active region, a lateral gradient can only be observed near the edge of the ridge.

Joule heating in most of the other layers outside the active region does not exceed the power value of 1 mW when injecting a current of 100 mA. The only exception is the InP-layer of the ridge generating a heat power up to 9 mW. Considering this additional source the maximum temperature of the active region increases by 0.6 K according to Fig. 3. In the following this third heat source will be neglected, justified by the fact that the contact heating is more than one order of magnitude greater.



Fig. 2 Calculated temperature distribution in a mounted laser diode structure (Isothermes) with two heat sources, (scheme of the structure with solder-metallization interface and the active layer is given only)



Fig. 3 Magnified part of Fig. 2 with the ridge region

Models of heat conduction problems often use the equivalent electrical method, replacing voltage, current and electrical resistance by temperature drop, heat flux and thermal resistance. The latter one is a parameter of the material, which is actually independent of the heat power value but not of the heat power distribution. In the simple case of only one uniform heat source in the active region the total thermal resistance of the laser chip mounted on the heat sink is given as

$$R_{th} \mid_{P_c = 0} = \Delta T_a / P_a \tag{6}$$

where $\Delta T_a = T_a \cdot T_s$. Without contact heating T_a reaches 31.7° only, resulting with (6) in a thermal resistance of 67 K/W. R_{th} describes the average thermal properties of all heat paths between the active region and the heat sink. The copper heat sink contributes an additional thermal resistance of about 5 K/W.

Influence of structural variations

In the following the dependence of the thermal resistance R_{th} on some structural modifications is demonstrated.

Table 2 Thermal resistance (6) for increasing ridge widths

ridge width w/µm	2	3	5	7
thermal resitance Rth/K/W	95	81	67	60

Table 2 shows that an increasing ridge width lowers the R_{th} -value because of greater starting areas of the heat conduction. Also the thickness and the conductivity of the solder layer exhibit a strong influence on the thermal resistance (see Fig. 4 and Fig. 5, resp.). If the solder conductivity value of 25



Fig. 4 Dependence of the thermal resistance R_{th} on the solder thickness d_1 , parameter is the ridge width w



Fig. 5 Dependence of the thermal resistance R_{th} on the thermal conductivity of the solder layer, parameter is the ridge width w



Fig. 6 Resonator length L dependence of the thermal resistance R_{th} , parameter is the ridge width w, the bars represent experimental results for $w = 2.7 \mu \text{m}$

W/Km is deteriorated by microscopic voids, for instance, a drastic increase of R_{th} may be caused, whereas the application of pure In-solder ($\lambda = 87$ W/mK) would lower the thermal resistance by about 20 K/W. Furthermore, the chip length L is an interesting parameter entering our model by the volume values in Eqs (4) and (5). Consequently an increasing length lowers the thermal resistance R_{th} with 1/L (Fig. 6).

Variations of some other structural parameters of the laser chip (substrate thickness, thicknesses of the etch stopping layer and the cap layer as well as the widths of the chip and the channels) by a factor of 2 change the thermal resistance no more than by 6% (see Fig. 12). The thicknesses of the InP-ridge [6] and the insulator layer have a similar small influence on the heat flux.

Table 3 Thermal resistance R_{th} of the chip mounted *p*-side up (a) with and (b) without a metallization window

ridge width	R _{th} /K/W		
w/µm	(a)	(b)	
2	163	158	
3	142	137	
5	121	116	
7	109	102	

Chip mounting p-side up

Mounting the chip with the InP-substrate down turns out as thermally disadvantegeous. Reasons therefore are the longer heat path and a metallization window for emission observation through the substrate as well as the fact that most of the contact heat flows through the active region.

Equivalent circuit analysis with two heat sources

In practice a high injection current I or a high ohmic resistance R_c of the contact lead to a significant contact heating. Considering a second heat source at the contact, Eq. (6) is no longer valid for transforming the calculated (or measured) temperature T_a into the thermal resistance R_{ih} and has to be replaced by a rather complex attempt. One part of the contact heat flows through the active region and the substrate to the heat sink, whereas the other part reaches the sink directly through the solder. Only the first path influences the temperature T_a of the active region. The relation of the two power parts depends on the thermal resistances of both heat paths from

the contact to the sink. At least three thermal resistances are needed in the equivalent circuit to describe this situation (Fig. 7). The known thermal resistance R_{th} of the total heat path from the active region to the sink is related to the resistances in Fig. 7 by

$$R_{th} = (R_1^{-1} + (R_2 + R_3)^{-1})^{-1}$$
(7)



Fig. 7 Equivalent thermal circuit of the OCMR laser diode

The corresponding temperature drop can be expressed by means of wiring diagram analysis

$$\Delta T_a = R_1 \left(P_a - \frac{R_1 P_a - R_3 P_c}{R_1 + R_2 + R_3} \right) \tag{8}$$

Eq. (8) allows a fitting to measured characteristics $T_a(I)$, if the thermal resistances R_1 , R_2 and R_3 in Fig. 7 are known. The ridge resistance R_2 is immediately given as

$$R_2 = \sum_i d_i / (w L \lambda_i) \quad (i = 3 - 6)$$
(9)

The resistances of the substrate (R_1) and the solder (R_3) are determined from calculation of the temperature T_a in two cases. On the one hand, R_{th} is obtained by Eq. (6) from the T_a -value without contact heating $(P_c = 0)$ and is then inserted into Eq. (7). On the other hand the computed result T_a leads in the case $P_a = P_c$ in Eq. (8) to an apparent thermal resistance R_{th}^* of $\Delta T_a/P_a$, which is equal to $\Delta T_a/P_c$. Thus, the unknown resistances R_1 and R_3 may be calculated by solving Eqs (7) and (8) as follows

$$R_3 = R_2 \left(R_{ih}^* - R_{ih} \right) / \left(2R_{ih} - R_{ih}^* \right)$$
(10)

$$R_1 = R_{th}^* \left(R_2 + R_3 \right) / \left(R_2 + 2R_3 - R_{th}^* \right) \tag{11}$$



Fig. 8 Dependence of the thermal resistances of the equivalent thermal circuit (Fig. 7) on the ridge width w

Making use of this procedure a substate thermal resistance $R_1 = 79$ K/W and a solder thermal resistance $R_3 = 279$ K/W are determined from the computed temperatures and the ridge thermal resistance $R_2 = 191$ K/W. The influence of different ridge width values is summarized in Fig. 8. The relations of the values $R_2 + R_3$ and R_1 in Fig. 8 show that more than 80 % of the heat generated inside the active region, flow through the substrate to the sink. Although this heat path is longer than the direct one through the ridge, it allows a greater heat flux area.

The thermal resistances R_1 , R_2 and R_3 lead according to Eq. (8) to the temperature rise ΔT_a for any other injection current I (see Fig. 10). The good agreement between these values and the results of PLTMG justifies the application of the equivalent circuit of Fig. 7.

A similar distinction of two heat paths has been published by Amann [5], neglecting the solder layer and assuming thermally isolated channels. The application of Amann's analytical relations to our case ($w = 5 \mu m$) would result in a substrate resistance R_1 of 67 K/W and a total resistance R_{th} of 50 K/W, which differ clearly from our results of 79 K/W and 67 K/W, respectively. Accordingly, Amann's model is not applicable to soldered laser chips.

Experimental investigation

The temperature rise in the InGaAsP/InP laser diode was determined by the temperature sensitivity of the voltage drop at the *p*-*n*-junction of the device.With increasing temperature the voltage drop lowers. When a constant current is applied there exists a linear dependence of both parameters.



Fig. 9 Temperature coefficient of the voltage drop at the *p*-*n*-junction of a InGaAsP/InP DHS vs. the drive current I at 300 K

The temperature coefficient dV/dT of the InGaAsP/InP DHS devices was measured by external heating. The result for a large current range is shown in Fig. 9.

When a fixed current is applied this coefficient can be used for the determination of the temperature rise in the device [7]. After switching on a loading current the voltage drops several mV due to heating. This voltage drop is supplied to one input of an operational amplifier. The second input is used for compensation. At the output the voltage transient can be observed giving an average temperature rise in the device.

$$\Delta T = -dT/dV \,\Delta V \tag{12}$$

To get some information about the distribution of the heat flux in the chip different mountings were investigated. Besides normal *p*-side-down mounting at the heatsink only half soldered laser diodes and laser diodes with a groove free of solder under ridge and channels were measured. So values of the equivalent circuit (Fig. 7) were determined experimentally. For a ridge width $w = 6 \mu m$ we got:

 $2 R_I = 156 - 164 \text{ K/W}, R_I = 80 - 82 \text{ K/W}, R_{th} = 55 - 61 \text{ K/W}$ (comp. Fig. 8) [8]. In further investigations the effect of various structure parameters on the temperature rise in the active region was studied.

Influence of contact resistance R_c and driving current I

The temperature rise in the active region versus the drive current can be calculated with the aid of the equivalent thermal circuit (Fig. 7), its parameters (Fig. 8) and Eq. (8). Figure 10 illustrates the influence of the contact resistance R_c for a ridge width $w = 2.8 \,\mu$ m. The experimental results fit well the temperature curve for a contact resistance $R_c = 4 \,\Omega$. The investigation of the V-I- characteristics of laser diodes from this wafer gave a resistance of 3-4 Ω . The calculated curves show that even small contact resistances yield a direct contribution to the active region heating at currents larger than 30 mA.

Influence of ridge width w and bonding properties

As theoretically and experimentally discussed the ridge itself carries only a small part of the whole heat flux. From a thermal point of view a large area is advantageous. But that contradicts the demand of light and current confinement. So a compromise must be found.



Fig. 10 Tempearture rise in the active region of a laser diode vs. the drive current, theoret. curves with $R_1 = 93$ K/W, $R_2 = 341$ K/W, $R_3 = 401$ K/W, o - exp. result for w = 2.8 μ m



Fig. 11 Dependence of the thermal resistance on the ridge width w for SnPbIn solder (a) and Indium solder (b), theoret. curves for $d_1 = 10/\mu m$, the bars represent the exp. results

The mounting technology for laser diodes is soldering with Indium and/or Tin solders or harder eutectic Gold solders. In Figs 4 and 5 we demonstrated already the effect of the thickness and the thermal conductivity of the solder layer. Experimentally the influence of ridge width w and solder material was investigated. Both pure Indium and a three component solder (Sn Pb29 In 18) were used. The thermal conductivities are 87 W/Km and 25 W/Km, respectively. The curves in Fig. 11 are calculated for a typical solder thickness of 10 μ m. The bars for the resistance values represent the variation of the solder thickness. The comparison of both solder materials results that the higher thermal conductivity of the pure Indium solder decreases the thermal resistance by about 20 K/W.

Mounting p-up or p-down at the heat sink

Because of simpler fibre coupling a p-side-up mounting was discussed. But because of the temperature problem this mounting has to be investigated from the thermal point of view, too. The theoretical and experimental results are reviewed in Table 4.

Mounting	R _{th} model	R _{th} exp
<i>p</i> -down	95	92-111
<i>p</i> -up	163	151-178

Table 4 Thermal resistance of *p*-down and *p*-up-mounted laser diodes, $w = 2\mu m$, structured contact

As already theoretically shown the p-up-mounting increases the thermal resistance of the laser diodes.

Laser diode length

As already shown the increase of the device length leads to a decrease of the thermal resistance. Because of the larger area the conditions for the heat dissipation improve. The results for various ridge widths w are presented in Fig. 6. The experimental results also show the 1/L decrease but not so steep as calculated. The reason for the small differences at longer device lengths L is that in the experiment the thermal resistance is referred to the total electrical power including losses at the contact. And as joule heating is stronger for smaller devices the thermal resistance lowers slightly.

Conclusion

The thermal resistance of InGaAsP/InP laser diodes with a ridgewaveguide structure was investigated both by a model and in experiments. The agreement of the results of modelling and experiment is very good. With the aid of the model a large number of parameter variations were investigated in a short time period. The investigation yields a lot of hints for the improvement of the structure and the mounting. Both theoretically and experimentally we showed that the bonding properties strongly affect the temperature rise in the active region. The influence of various parameters on the thermal resistance with a factor-of-2-variation is presented in Fig. 12. While the influence of substrate thickness or channel width is very low (small gradient) the device length L and the ridge width w show the strongest effect. If several parameters are changed the alteration of the ther-



Fig. 12 Factor-of-two variation of several structure parameters (normalized to the values of Table 1) affecting the thermal resistance, $R_0 = 67$ K/W. a - solder thickness; b - thickness of the etch stop layer; c - thickness of the contact layer; d - channel width C; e - substrate thickness; f - chip width; g - thermal conductivity of the solder; h - ridge width w; i - device length L

mal resistance results approximately by the multiplication of the single factors of the variations.

References

- 1 H. J. Bachert, J. Frahm, R. Puchert, K. Vogel and G. Wagner, 3. Internat. Conference on Trends in Quantum Electronics Bucharest, 1988, p. 99
- 2 W. Both and R. Schließer, Schweißtechnik, 37 (1987) 111.
- 3 W. Both, V. Gottschalch and G. Wagner, Cryst. Res. Technol., 21 (1986) 87.
- 4 R. E. Balk, PLTMG User's guide, Version 6/81. University of California at San Diego, Depart. Math., La Jolla, California (1982)
- 5 M.-C. Amann, Appl. Phys. Lett., 5 (1987) 4.
- 6 J. Piprek and R. Nürnberg, Kvant. Electron., 15 (1988) 2249.
- 7 W. Both, Z. elektr. Inform.-u. Energietechnik, 12 (1982) 558.
- 8 W. Both and W. Nakwaski, Thermal resistance of InGaAsP/InP laser diodes. Internat. Conf. on Semiconductor Injection Lasers SELCO'87, Holzhau/DDR, (1987) p. 9.

Zusammenfassung — Die Ergebnisse einer theoretischen und experimentellen Untersuchung des thermischen Verhaltens von InGaAsP/InP Laserdioden mit Stegwellebleiterstruktur wurden dargelegt. Es wurde gezeigt, daß der größte Teil des Wärmeflusses durch das InP-Substrat geleitet wird, nur weniger als 1/4 durch den Steg. Man bestimmte den Temperaturanstieg in der aktiven Zone und berechnete für verschiedene Struktur- und Montageparameter die thermische Widerstand. Theoretische und experimentelle Ergebnisse stimmen gut miteinander überein. Die Änderung der thermischen Beständigkeit verglichen mit einem Normwert von 67 K/W wird in Abhängigkeit der Strukturparameter untersucht. Sie wird durch chiplänge Stegbreite und Bindungsparameter stark beeinflußt.